REMARKS

This Amendment is filed in response to the Office Action dated August 27, 2007, which has a shortened statutory period set to expire November 27, 2007. A request for a two month extension of time is provided herewith, thereby allowing Applicant to respond by January 28, 2008.

Claims 37 and 41-59 Are Patentable Over Chou

Claim 37, as amended, recites in part:

> wherein the first memory request further includes memory mapped I/O addresses in the header, the memory mapped I/O addresses comprising a command word port and a data value port.

Applicant respectfully submits that Chou fails to teach these limitations. The First Office Action cites FIGS. 5-8 as teaching these limitations (which were formerly recited in Claims 39 and 40). Applicant traverses this characterization. Specifically, FIG. 5 illustrates a transaction-layer packet (col. 2, line 47); FIG. 6 illustrates a table of transaction-layer packet types used for communicating with the serial flash-memory chip (col. 2, lines 48-49); FIG. 7 illustrates a table of request and response packets used for various flash-memory commands (col. 2, lines 50-51); and FIG. 8 illustrates a generic format for a vendor-defined message packet (col. 2, lines 52-53). Notably, these figures and their associated descriptions do not teach that the first memory request further includes memory mapped I/O addresses, i.e. the command word port and the data value port.

As taught by Applicant in the Specification (emphasis added), these memory mapped I/O addresses provide significant advantages.

[0122] … host controller 1003 can assign resources, e.g. configuration base addresses associated with flash device 1002. In one embodiment, flash controller 1004 can ask host 1001 during the configuration process to assign these resources and, to facilitate this assignment, can inform host 1001 how much of these resources are needed. Of importance, flash controller 1004 can ask for as few as three base addresses, thereby saving valuable system memory space. **These configuration base addresses include a command word port, a sector data value port, and a register value port.** For example, in one embodiment, BIOS could assign a 32-bit address to these ports by writing FFFF,FFFFh to flash device 1002. At this point, logic in flash controller 1004 should return FFFF,FFFCh to tell BIOS that it is a 32-bit address. Flash device 1002 should latch this base address during the configuration process after system resources are assigned to each PCI Express device.

[0123] **These ports advantageously are memory-mapped IO addresses. Therefore, host controller 1003 can write, read, and erase flash memory modules 1006 as if this flash memory were part of the storage system of host device 1001. Note that this memory mapping technique eliminates the need for an I/O transaction, which is used in a standard PCI Express operation.** Flash controller 1004 can use the memory mapped I/O address, which is provided in field 305 (Figure 3), to identify a command and a sector data transfer.

FIG. 9 of Chou illustrates a header for a memory-request packet. Col. 2, line 53. Notably, the description of the address field of this header teaches nothing about memory-mapped I/O addresses.

Because Chou fails to disclose or suggest that the memory request includes memory mapped I/O addresses in the header, wherein the memory mapped I/O addresses comprises a command word port and a data value port, Applicant respectfully requests reconsideration and withdrawal of the rejection of Claim 37.

Claims 41-59 depend from Claim 37 and therefore are patentable for at least the reasons presented for Claim 37.

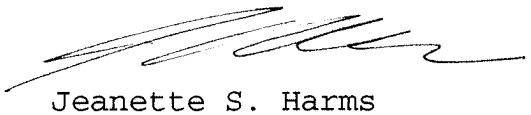
Based on those reasons, Applicant requests reconsideration and withdrawal of the rejection of Claims 41-59.

CONCLUSION

Claims 37 and 41-59 are pending in the present application. Allowance of these claims is respectfully requested.

If there are any questions, please telephone the undersigned at 408-451-5907 to expedite prosecution of this case.

Respectfully submitted,



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